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# FEE TRANSMITTAL
## For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

| TOTAL AMOUNT OF PAYMENT | ($) 500.00 |
|---|---|

| *Complete If Known* | |
|---|---|
| Application Number | 09/978,528-Conf. #5054 |
| Filing Date | October 17, 2001 |
| First Named Inventor | Andres Bryant |
| Examiner Name | A. N. Sefer |
| Art Unit | 2826 |
| Attorney Docket No. | 21806-00142-US1 |

**METHOD OF PAYMENT** (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 09-0456 Deposit Account Name: IBM Corporation (Burlington)

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| Application Type | Fee ($) | Small Entity Fee ($) | Fee ($) | Small Entity Fee ($) | Fee ($) | Small Entity Fee ($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | |

**2. EXCESS CLAIM FEES**

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 50 | 25 |
| Each independent claim over 3 (including Reissues) | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 20 = | _____ | x _____ | = _____ |

| Indep. Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 3 = | _____ | x _____ | = _____ |

| Multiple Dependent Claims | |
|---|---|
| Fee ($) | Fee Paid ($) |
| _____ | _____ |

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee ($) | Fee Paid ($) |
|---|---|---|---|---|
| _____ - 100 = | _____ / 50 | _____ (round up to a whole number) x | _____ | = _____ |

**4. OTHER FEE(S)** **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount)

Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal 500.00

| SUBMITTED BY | | | | | |
|---|---|---|---|---|---|
| Signature | Larry J. Hume | Registration No. (Attorney/Agent) | 44,163 | Telephone | (202) 331-7111 |
| Name (Print/Type) | Larry J. Hume | | | Date | February 21, 2006 |

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# FAX TRANSMISSION

**DATE:** February 21, 2006

**PTO IDENTIFIER:** **Application Number** 09/978,528-Conf. #5054
**Patent Number**

**Inventor:** Andres Bryant et al.

**MESSAGE TO:** US Patent and Trademark Office

**FAX NUMBER:** (571) 273-8300

**FROM:** CONNOLLY BOVE LODGE & HUTZ LLP
Larry J. Hume
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**Attorney Dkt. #:** 21806-00142-US1

**PAGES (Including Cover Sheet):** 29

**CONTENTS:**
Appeal Brief Transmittal (1 page)
Fee Transmittal (1 page)
Appeal Brief (25 pages)
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Application No. (if known): 09/978,528 Attorney Docket No.: 21806-00142-US1

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Typed or printed name of person signing Certificate

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Appeal Brief (25 pages)

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| TRANSMITTAL OF APPEAL BRIEF | | | Docket No. 21806-00142-US1 |
|---|---|---|---|
| In re Application of: Andres Bryant et al. | | | |
| Application No. 09/978,528-Conf. #5054 | Filing Date October 17, 2001 | Examiner A. N. Sefer | Group Art Unit 2826 |
| Invention: DISPOSABLE SPACER FOR SYMMETRIC AND ASYMMETRIC SCHOTTKY CONTACT TO SOI MOSFET FOR CONTROLLING THE BODY POTENTIAL | | | |

**TO THE COMMISSIONER OF PATENTS:**

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: December 19, 2005 .

The fee for filing this Appeal Brief is $ 500.00 .

[x] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[x] Charge the amount of the fee to Deposit Account No. 09-0456 .
This sheet is submitted in duplicate.

[ ] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 09-0456 .
This sheet is submitted in duplicate.

Larry J. Hume

Dated: February 21, 2006

Larry J. Hume
Attorney Reg. No.: 44,163
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Docket No.: 21806-00142-US1
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Andres Bryant et al.

Confirmation No.: 5054

Application No.: 09/978,528

Filed: October 17, 2001

Art Unit: 2826

For: DISPOSABLE SPACER FOR SYMMETRIC AND ASYMMETRIC SCHOTTKY CONTACT TO SOI MOSFET FOR CONTROLLING THE BODY POTENTIAL

Examiner: A. N. Sefer

# APPEAL BRIEF

**MS Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**February 21, 2006 (Tuesday)**

Dear Sir:

As required under § 41.37(a), this brief is timely filed within two months of the Notice of Appeal filed in this case on December 19, 2005, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

| | |
|---|---|
| I. | Real Party In Interest |
| II | Related Appeals and Interferences |
| III. | Status of Claims |
| IV. | Status of Amendments |
| V. | Summary of Claimed Subject Matter |
| VI. | Grounds of Rejection to be Reviewed on Appeal |
| VII. | Arguments |



PAGE 5/29 * RCVD AT 2/21/2006 7:33:08 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/37 * DNIS:2738300 * CSID:202 293 6229 * DURATION (mm-ss):07-32

02/23/2006 EFLORES 00000038 090456 09978528
01 FC:1402 500.00 DA

Application No.: 09/978,528 Docket No.: 21806-00142-US1

| | |
|---|---|
| App. A | Claims on Appeal |
| App. B | Evidence |
| App. C | Related Proceedings |



## I. REAL PARTY IN INTEREST

Real party in interest: International Business Machines Corporation, Armonk, NY USA.

## II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## III. STATUS OF CLAIMS

A. Total Number of Claims in Application: There are 10 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: 1-22, 26, and 32-33

2. Claims withdrawn from consideration but not canceled: none

3. Claims pending: 23-25, 27-31, and 34-35

4. Claims allowed: None

5. Claims rejected: 23-25, 27-31, and 34-35

C. Claims On Appeal: The claims on appeal are claims 23-25, 27-31, and 34-35.

## IV. STATUS OF AMENDMENTS

Applicant filed an Amendment After Final Rejection on September 30, 2005 via the Express Mail procedure. The Examiner refers to the September 30, 2005 Amendment after Final as being filed on October 3, 2005, a date that was likely the USPTO receipt date of the mailing.

However, even though the amendment to the claims was directed to incorporating the subject matter of previously examined dependent claim 35 into independent claim 34, the Examiner inexplicably refused entry of the Amendment after Final, except to assert that Applicants' distinguishing arguments over the applied art were not persuasive.

Therefore, the claims on appeal in Appendix A do not include the claim amendments after final proffered by Appellants, but do include the amendments made in the "Second Resubmission of Amendment" filed by the Express Mail procedure on April 12, 2005.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

### A. Overview of Applicants' Claimed Invention

A "plain-language" overview of the claimed subject matter and related background information is provided to aid in the Honorable Board's understanding of the unique and non-obvious aspects of Applicants' invention.

Applicants have developed a structure for minimizing floating body effects of an SOI device using a Schottky contact to the source and/or drain is formed to reduce the charge accumulated in the body of the transistor.

A Schottky diode and its resulting "barrier" results in both very fast switching times and low forward voltage drop. The Schottky diode is a "majority carrier" semiconductor device. This means that if the semiconductor body is doped N-type, only the N-type carriers (mobile electrons) play a significant role in normal operation of the device. No slow, random recombination of N- and P- type carriers is involved, so this diode can cease conduction faster than an ordinary PN rectifier diode. This property in turn allows a smaller device area, which also makes for a faster transition.

In this application, the Schottky contact is formed (using disposable spacers) in such a way that the Schottky contact is self aligned. The Schottky diode enhances the forward bias leakage of the transistor, and will hold the body of the transistor at a lower voltage potential than

it would otherwise be. Thus, the range of body voltages of the transistor is more narrowly bounded, resulting in better accommodation of higher burn-in voltages during production testing by keeping the body charge low, and normal operation of the device during burn-in.

**B. Detailed Summary of Claimed Invention with Reference to the Disclosure**

A detailed cross-reference to the Specification and Replacement Drawing Figures is provided below using paragraph numbering as published in U.S. Patent Application Publication US 2002/0048841A1 (this application). This detailed summary is provided below as required by the Patent Rules with respect to embodiments claimed in independent claims 23 and 34.

In one embodiment, a semiconductor device includes a semiconductor layer 10 formed on an insulating layer 8, and a gate conductor 12 formed on the semiconductor layer 10. (See Specification at paragraph [0013] and FIGS. 2-7). Spacers 18 are formed on sidewalls 14 of the gate conductor 12 and on the semiconductor layer 10. (See Specification at paragraph [0013] and FIG. 4). Extension regions 16 are arranged in the semiconductor layer 10 on both sides of the gate conductor 12 and extend under and contact the spacers 18 and a portion of the gate conductor 12. (See Specification at paragraph [0015] and FIGS. 4-7). A portion 17 of at least one of the extension regions 16 is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers. (See Specification at paragraph [0020] and FIG. 6). Diffusion regions 20 are formed in the semiconductor layer 10 adjacent to the extension regions 16. (See Specification at paragraph [0016] and FIGS. 5-7). A metal layer 22 is formed at least in the exposed portion 17 of the extension region 16, and the metal layer 22 contacts the semiconductor layer (10/21) and the exposed portion 17 of the extension region 16. (See Specification at paragraph [0020] and FIG. 7).

In another aspect of this embodiment, an integrated circuit is disposed on an SOI substrate. (See FIGS. 2-7). The integrated circuit has a body region 21 that includes a transistor having a source diffusion region (20, left-hand side of FIGS. 6-7), a gate 12 formed over the body region 21, a first sidewall spacer 14 disposed on a sidewall of the gate 12 abutting the source diffusion region (20, left-hand side of FIGS. 6-7), a drain diffusion region (20, right-hand

side of FIGS. 6-7), a second sidewall spacer 18 disposed on a sidewall 14 of the gate 12 abutting the drain diffusion region (20, right-hand side of FIGS. 6-7). The first sidewall spacer is thinner than the second sidewall spacer. (See FIGS. 6-7). Extension regions 16 are provided under and in contact with the first (14) and second sidewall spacers (14/18). (See Specification at paragraph [0015] and FIGS. 6-7). The extension regions 16 contact the gate 12 and extend further under the gate than the source and drain diffusion region 20. (See Specification at paragraphs [0014] and [0016] and FIGS. 6-7). A portion 17 of at least one of the extension regions 16 is exposed at a surface 17 of the body region 21 by removing at least a part of one of the first and second sidewall spacers 14/18. A conductor 22 is formed at least in the exposed portion 17 of the extension region 16. (See Specification at paragraph [0020] and FIG. 6). The conductor 22 is in contact with the exposed portion 17 of the extension region 16 and at least a portion of the source diffusion region 20, thus forming a Schottky diode (See Specification at paragraph [0020] and FIGS. 6-7).

## VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

**A. 35 U.S.C. 103(a) Rejection of claims 23-25 and 27-29 over Deleonibus (US 6,091,076) in view of Koh (US 6,049,110)**

**B. 35 U.S.C. 103(a) Rejection of claims 23-25 and 27-31 over Yamaguchi et al. (US 5,341,028) in view of Imai (US 6,297,529) and Koh (US 6,049,110)**

**C. 35 U.S.C. 103(a) Rejection of claim 34 over Yamaguchi et al. (US 5,341,028) in view of Gardner et al. (US 6,096,615) and Koh (US 6,049,110)**

**D. 35 U.S.C. 103(a) Rejection of claim 35 over Yamaguchi et al. (US 5,341,028) in view of Gardner (US 6,096,615), Koh (US 6,049,110), and Imai (US 6,297,529)**

**E. 35 U.S.C. 103(a) Rejection of claim 34 under 35 U.S.C. 103(a) over Deleonibus (US 6,091,076) in view of Gardner (US 6,096,615) and Koh (US 6,049,110)**

**F. 35 U.S.C. 103(a) Rejection of claim 35 under 35 U.S.C. 103(a) over Deleonibus (US 6,091,076) in view of Gardner (US 6,096,615) and Koh (US 6,049,110) and Imai (US 6,297,529)**

## VII. ARGUMENT

### A. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claims 23-25 and 27-29 over Deleonibus (US 6,091,076) in view of Koh (US 6,049,110).

#### 1. The applied art does not teach or suggest all the claim limitations

The conventional transistors illustrated in Deleonibus FIGS. 1 and 2 are offered by the Examiner as teaching n-type diffused areas (8, 10) (less doping than in areas 4 and 6) as extension regions, and polycrystalline silicon layer (20) as a gate conductor.

However, as shown in FIG. 1 of Deleonibus (reproduced below), extension regions (8, 10) do not ***extend under and contact*** electrically insulating spacers (24, 26) ***and a portion of the gate conductor*** (20). Rather, a grid insulation layer (18) is interposed between extension regions (8, 10) and spacers (24, 26) and gate conductor (20), thus precluding contact between the extension regions and the spacers. The Examiner admits this deficiency of Deleonibus.

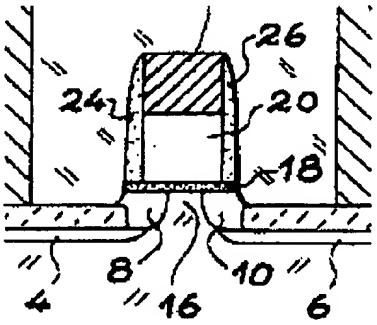



FIG. 1

In contrast to Deleonibus, the invention recited in claims 23-25 and 27-33 comprises a combination of elements, including extension regions extending under and contacting spacers and a portion of a gate conductor, along with a metal layer that contacts the semiconductor layer and the extension region.

To make up for the admitted deficiency of Deleonibus, the Examiner offers Koh FIG. 43 (reproduced below)as teaching "a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor."

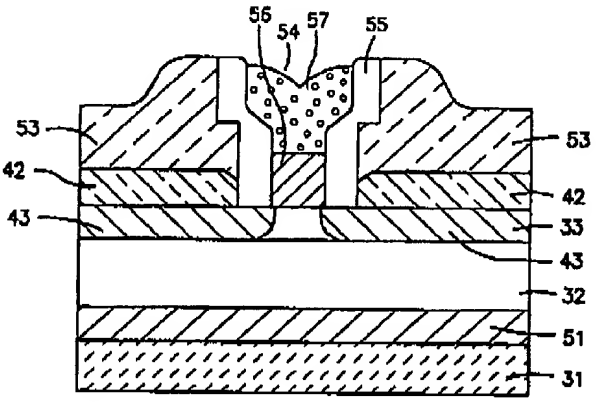



FIG. 43

Appellants respectfully disagree with the Examiner's characterization of Koh.

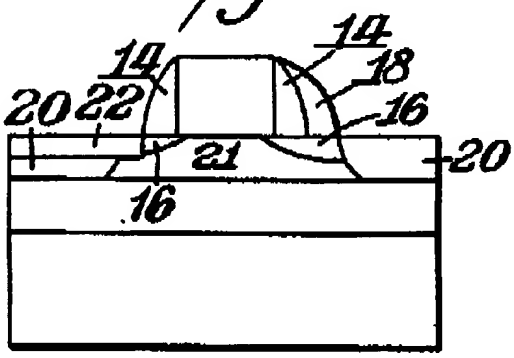
What the "regions under reference numerals 55 and 56" actually disclose are the ***source and drain regions 43 of Koh's device***, *i.e.*, diffusion regions. Koh's source/drain regions 43 actually appear to read on Appellants' recited "diffusion regions formed in the semiconductor layer adjacent to the extension regions", and are clearly not, in any fair interpretation, "extension regions". Koh further does not teach or suggest a metal layer that contacts both the semiconductor layer and an extension region.

In particular, the applied art, either alone or in combination, does not teach or suggest a semiconductor device that includes, among other features, "...extension regions arranged in the semiconductor layer on both sides of the gate conductor and ***extending under and contacting the spacers and a portion of the gate conductor***, wherein a portion of at least one of the extension

regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers...and ***a metal layer...contacting the semiconductor layer and the...extension region***...", as recited in independent claim 23 (emphasis added).

In support of Appellants' position, Appellants offer FIG. 7 of the present application, reproduced below. FIG. 7 illustrates these features, *i.e.*, that extension regions 16 extend under and make contact with spacers 14 and gate conductor 12 (not labeled in FIG. 7, but see FIG. 2), and that metal layer 22 contacts both the semiconductor layer and the extension region.

Fig. 7.




Since none of the references relied upon in the Office Action teach or suggest extension regions extending under and contacting spacers and a portion of a gate conductor, along with a metal layer contacting the semiconductor layer and the extension region as recited in independent claim 23, Applicants believe that each of pending claims 23-25 and 27-31 are patentably distinguishable over the suggested combination of Deleonibus and Koh.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of these claims by the Honorable Board are respectfully requested.

**2. The Examiner has not provided the proper motivation to combine the references in the manner suggested.**

The Examiner has not met his burden in establishing a *prima facie* case of unpatentability by failing to establish the proper motivational basis for combining Deleonibus with Koh in the manner suggested.

In particular, and although Deleonibus and Koh may both be generally related to semiconductor devices, Deleonibus FIG. 1 is seen to not be reasonably related to SOI MOSFET devices, to which Appellants' disclosure is clearly drawn. Instead, Deleonibus is directed to a quantum well MOS transistor that has an insulating layer thin enough to enable passage of charge carriers by the tunneling effect.

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.[1] Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.[2]

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."[3] Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.[4] The level of skill in the art cannot be relied upon to provide the suggestion to combine references.[5]

Being generally related to "MOS transistors" is submitted as not being sufficient to motivate a person with skill in the art to combine the references in the manner suggested. The problems to be solved by Deleonibus, Koh, and Appellants' claimed invention are not

[1] *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)
[2] *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)
[3] *See* MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).
[4] *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).
[5] *See* MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

sufficiently related in terms of the problems solved to provide the proper motivation to a person with skill in the art. Any attempt to assert such motivation appears to invoke improper hindsight analysis, using Appellants' disclosure against them.

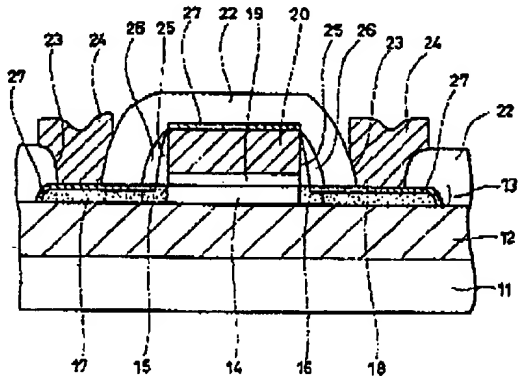
Accordingly, even assuming, *arguendo*, that the applied art contains all the limitations, Appellants submit that there is no motivation to combine the references in the manner suggested by the Examiner.

**B. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claims 23-25 and 27-31 over Yamaguchi et al. (US 5,341,028) in view of Imai (US 6,297,529) and Koh.**

**1. The applied art does not teach or suggest all the claim limitations**

The Office Action construed regions (15, 16) of Yamaguchi et al. as extension regions and gate electrode (20) as a gate conductor. However, as shown in Fig. 5 of Yamaguchi et al. (reproduced below), extension regions (15, 16) do not extend under and contact a portion of the gate conductor (20).

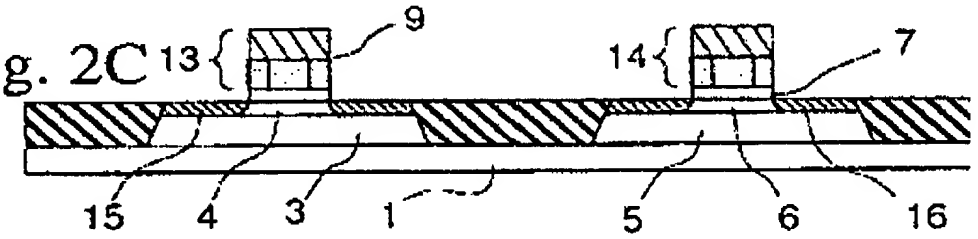
FIG. 5




The Examiner admits this deficiency of Yamaguchi et al., and instead offers Imai as making for this deficiency by construing regions (16) of Imai as extension regions, layers (14) as a gate conductor, and N well 5/PMOS channel 6 as the claimed "semiconductor layer".

However, as shown in Fig. 2C of Imai (reproduced below), what the Examiner offers as extension regions (16) do not extend under and contact a portion of the gate conductor (14).

Fig. 2C




The Examiner also improperly construes lightly doped drain (LDD) region 16 of Imai as an extension region. Similar to the discussion above with respect to Koh, region 16 acts as a source/drain (diffusion) region, and may not reasonably be construed as an extension region, as claimed.

Further, the Examiner goes on to erroneously assert that silicide layer 20 (See FIG. 2F of Imai, below) teaches "a metal layer 20 formed at east in the exposed portion of the extension region and extending into the semiconductor layer (as in claim 30) or extends into a portion of the semiconductor layer below said extension region (as in claim 31), the metal layer contacting the semiconductor layer and the exposed portion of the extension region."

Fig. 2F

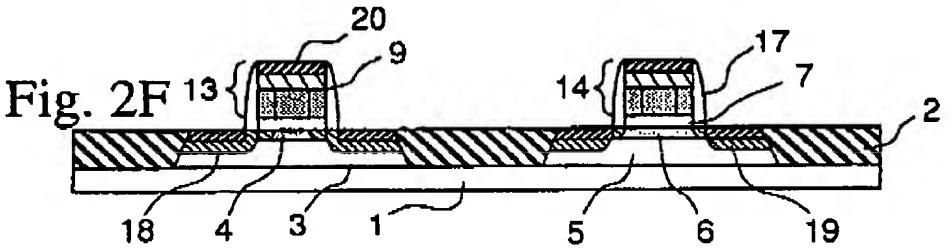



FIG. 2F of Imai actually discloses a dual gate NMOS/PMOS device having a layered gate structure that has a lowermost layer of the gate doped with an impurity, and where the upper gate layers are undoped.

Silicide layer 20 of Imai merely constitutes a portion of the gate structure for the NMOS device. At a minimum, silicide layer 20 does not extend into the semiconductor layer, as claimed.

The Examiner goes on to assert that Koh FIG. 43 as teaches "a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor."

Appellants again respectfully disagree with the Examiner's characterization of Koh.

As mentioned above, what the "regions under reference numerals 55 and 56" actually disclose are the ***source and drain regions 43 of Koh's device***, *i.e.*, diffusion regions. Koh's source/drain regions 43 actually appear to read on Appellants' recited "diffusion regions formed in the semiconductor layer adjacent to the extension regions", and are clearly not, in any fair interpretation, "extension regions". Koh further does not teach or suggest a metal layer that contacts both the semiconductor layer and an extension region.

Since none of the references relied upon in the Office Action teach or suggest extension regions extending under and contacting spacers and a portion of a gate conductor, along with a metal layer contacting the semiconductor layer and the extension region as recited in independent claim 23, Applicants believe that each of pending claims 23-25 and 27-31 are patentably distinguishable over the suggested combination of Yamaguchi, Imai, and Koh.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of these claims by the Honorable Board are respectfully requested.

**2. The Examiner has not provided the proper motivation to combine the references in the manner suggested.**

Again, even assuming, *arguendo*, that the suggested combination teaches or suggest all the claimed limitations of independent claim 23, a proposition with which Appellants vigorously disagree, the Examiner has still not made a *prima facie* case of unpatentability by his failure to establish the proper motivational basis for combining the references in the manner suggested.

The Examiner improperly asserts that it would have been obvious to one skilled in the art "to incorporate Imai's teachings with Yamaguchi's device since that would prevent an increase of the contact resistance of the gate electrode with the metal layer." The Examiner also erroneously asserts that "[i]t would be obvious to incorporate Koh's teachings since that would suppress short channel effects as taught by Koh."

Why such modifications would be "obvious" in the context of Appellants' disclosure directed to minimizing floating body effects in SOI devices is not explained by the Examiner. The applied art all solve different technical problems, different still from the problem solved by Appellants' disclosure.

Appellants are not necessarily concerned with either preventing an increase of the contact resistance of the gate electrode with the metal layer, or in suppressing short channel effects, as is the combination of art applied by the Examiner.

Accordingly, Appellants submit that there is no motivation to combine the references in the manner suggested by the Examiner.

**C. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claim 34 over Yamaguchi in view of Gardner et al. (US 6,096,615) and Koh.**

**1. The applied art does not teach or suggest all the claim limitations**

The Examiner offers Yamaguchi FIGS. 5 and 6 as disclosing most limitations of independent claim 34, but admits that Yamaguchi is deficient at least in two respects.

First, the Examiner admits that Yamaguchi is deficient in disclosing that a first sidewall spacer is thinner than a second sidewall spacer, and second, that Yamaguchi is deficient in disclosing extension regions under and contacting first and second sidewall spacers and which contact the gate region and extend further under the gate or a first sidewall spacer thinner than a second sidewall spacer.

The Examiner offers Gardner et al. as disclosing the first deficient feature of Yamaguchi, *i.e.*, a first sidewall spacer that is thinner than a second sidewall spacer, and refers to Gardner et al. FIG. 2G and col. 5, lines 1-15 in support thereof.

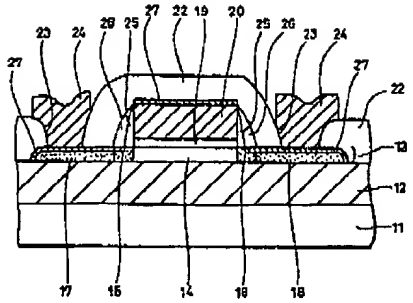
The Examiner offers Koh FIG. 43 as teaching "a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension diffusion regions (regions under reference numerals 55 and 56) provided under and contacting first and second sidewall spacers 55, said extension diffusion regions contacting said gate and extending further under the gate conductor 56 and extending further under said gate conductor."

What the "regions under reference numerals 55 and 56" actually disclose are the ***source and drain regions 43 of Koh's device***. Koh's source/drain regions 43 actually appear to read on Appellants' separately recited "source diffusion region" and "drain diffusion region" formed adjacent to the claimed "extension regions", and are clearly not, in any fair interpretation, "extension regions".

Appellants further point out that the Examiner's assertion that Yamaguchi discloses "a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode" is completely unsupported by the disclosure of Yamaguchi.

Specifically, Yamaguchi FIG. 5 (reproduced below) and at col. 6, lines 1-66. discloses that metal layer 27 is formed on gate electrode 20, as shown below.

FIG. 5




Metal layer 27 does not contact either an extension region or the source diffusion region. Further, Yamaguchi is completely silent on formation of a Schottky diode, as claimed. Clearly, Yamaguchi is completely deficient and does not teach or suggest that for which it is offered by the Examiner.

In particular, the applied art, either alone or in combination, does not teach or suggest an integrated circuit disposed on an SOI substrate having a body region, which includes, among other features, "...extension regions provided under and contacting the first and second sidewall spacers, the extension regions contacting the gate and extending further under the gate than the source and drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region by removing at least a part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode", as recited in independent claim 34.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of claim 34 by the Honorable Board are respectfully requested.

**2. The Examiner has not provided the proper motivation to combine the references in the manner suggested.**

In particular, and although Yamaguchi, Gardner, and Koh are may generally be related to semiconductor devices, Gardner is seen to not be reasonably related to SOI MOSFET devices, to which Appellants' disclosure is clearly drawn. Instead, Gardner is directed to a method of forming a semiconductor device having a narrow gate electrode, and appears to be completely unrelated to SOI devices.

Being generally related to "MOS transistors" is submitted as not being sufficient to motivate a person with skill in the art to combine the references in the manner suggested. The problems to be solved by Yamaguchi, Gardner, Koh, and Appellants' claimed invention are not sufficiently related in terms of the problems solved to provide the proper motivation to a person with skill in the art. Any attempt to assert such motivation appears to invoke improper hindsight analysis, using Appellants' disclosure against them.

Particularly, none of the references suggested for combination by the Examiner deals with Appellants' technical problem of floating body effects in SOI devices.

Accordingly, Appellants submit that there is no motivation to combine the references in the manner suggested by the Examiner.

**D. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claim 35 over Yamaguchi in view of Gardner, Koh, and Imai**

In the interests of brevity, Appellants will not belabor the deficiencies of the suggested combination, except to note that Imai does not make up for the previously identified deficiencies of Yamaguchi, Gardner, and Koh, discussed above with respect to independent claim 34, from which claim 35 depends.

Not only does the suggested combination not teach or suggest all the claim limitations, Imai likewise does not provide a basis for proper motivation to combine the references in the manner suggested.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of claim 35 by the Honorable Board are respectfully requested.

**E. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claim 34 under 35 U.S.C. 103(a) over Deleonibus in view of Gardner and Koh**

**1. The applied art does not teach or suggest all the claim limitations**

The Examiner offers Deleonibus FIG. 2 as disclosing most of the limitation of independent claim 34, but admits that Deleonibus does not teach or suggest "extension regions provided under and contacting first and second sidewall spacers, the extension regions contacting said gate and extending further under the gate or a first sidewall spacer thinner than a second sidewall spacer."

The Examiner offers Gardner FIG. 2G and col. 5, lines 1-15 as disclosing a first sidewall spacer 210 thinner than a second sidewall spacer 219.

The Examiner goes on to assert that Koh FIG. 43 as teaches "a semiconductor device comprising a semiconductor layer formed on an insulating layer 31 including extension regions (regions under reference numerals 55 and 56) extending further under the spacers 55 arranged in the semiconductor layer on both sides of a gate conductor 56 and extending under and contacting the spacers and a portion of the gate conductor."

Appellants again respectfully disagree with the Examiner's characterization of Koh.

As mentioned above, what the "regions under reference numerals 55 and 56" actually disclose are the ***source and drain regions 43 of Koh's device***, *i.e.*, diffusion regions. Koh's

source/drain regions 43 would better read on Appellants' recited source and drain diffusion regions, and are clearly not, in any fair interpretation, "extension regions", as disclosed and claimed.

Further, ***none*** of the applied art even remotely mentions formation of a Schottky diode, as claimed.

In particular, the applied art, either alone or in combination, does not teach or suggest an integrated circuit disposed on an SOI substrate having a body region, which includes, among other features, "...extension regions provided under and contacting the first and second sidewall spacers, the extension regions contacting the gate and extending further under the gate than the source and drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region by removing at least a part of one of the first and second sidewall spacers; and a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode", as recited in independent claim 34.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of claim 34 by the Honorable Board are respectfully requested.

**2. The Examiner has not provided the proper motivation to combine the references in the manner suggested.**

Being generally related to "MOS transistors" is submitted as not being sufficient to motivate a person with skill in the art to combine the references in the manner suggested. The problems to be solved by Deleonibus, Gardner, Koh, and Appellants' claimed invention are not sufficiently related in terms of the problems solved to provide the proper motivation to a person with skill in the art. Any attempt to assert such motivation appears to invoke improper hindsight analysis, using Appellants' disclosure against them.

Particularly, none of the references suggested for combination by the Examiner deals with Appellants' technical problem of floating body effects in SOI devices.

Accordingly, Appellants submit that there is no motivation to combine the references in the manner suggested by the Examiner.

**F. The Examiner has not met his burden in establishing a *prima facie* case of unpatentability in the rejection of claim 35 under 35 U.S.C. 103(a) over Deleonibus in view of Gardner, Koh, and Imai**

In the interests of brevity, Appellants will not belabor the deficiencies of the suggested combination, except to note that Imai does not make up for the previously identified deficiencies of Deleonibus, Gardner, and Koh, discussed above with respect to independent claim 34, from which claim 35 depends.

Not only does the suggested combination not teach or suggest all the claim limitations, Imai likewise does not provide a basis for proper motivation to combine the references in the manner suggested.

Accordingly, since the applied art does not teach or suggest all the claimed limitations, reversal of the rejections and allowance of claim 35 by the Honorable Board are respectfully requested.

## VIII. CLAIMS

A copy of claims 23-25, 27-31, and 34-35 involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do not include the amendments after final rejection mailed by Applicant on September 30, 2005, which were not entered by the Examiner.

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In view of the Arguments presented above, reversal of the rejections by the Honorable Board and allowance of all pending claims 23-25, 27-31, and 34-35 are respectfully requested.

Respectfully submitted,

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## APPENDIX A- CLAIMS ON APPEAL

**Claims Involved in the Appeal of Application Serial No. 09/978,528**

23. A semiconductor device comprising:

a semiconductor layer formed on an insulating layer;

a gate conductor formed on the semiconductor layer;

spacers formed on sidewalls of the gate conductor and on the semiconductor layer;

extension regions arranged in the semiconductor layer on both sides of the gate conductor and extending under and contacting the spacers and a portion of the gate conductor, wherein a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer by removing at least a part of one of the spacers;

diffusion regions formed in the semiconductor layer adjacent to the extension regions; and

a metal layer formed at least in the exposed portion of the extension region, the metal layer contacting the semiconductor layer and the exposed portion of the extension region.

24. The device according to claim 23, wherein the extension regions are lower doped than the diffusion regions.

25. The device according to claim 23, wherein the metal layer contacts at least one of the diffusion regions.

27. The device according to claim 23, wherein a portion of each extension region is exposed on both sides of the gate conductor at the surface of the semiconductor layer by removing at least a portion of each spacer and the metal layer is formed in the exposed portions of the extension regions.

28. The device according to claim 23, wherein the extension regions extend further under the spacers than the diffusion regions.

29. The device according to claim 23, wherein the metal layer and the exposed portion of the extension region form a Schottky diode.

30. The device according to claim 29, wherein the metal layer extends into the semiconductor layer.

31. The device according to claim 30, wherein the metal layer extends into a portion of the semiconductor layer below the extension regions.

34. An integrated circuit disposed on an SOI substrate having a body region, comprising:

a transistor having

a source diffusion region,

a gate formed over the body region,

a first sidewall spacer disposed on a sidewall of the gate abutting the source diffusion region,

a drain diffusion region,

a second sidewall spacer disposed on a sidewall of the gate abutting the drain diffusion region, wherein the first sidewall spacer is thinner than the second sidewall spacer, and

extension regions provided under and contacting the first and second sidewall spacers, the extension regions contacting the gate and extending further under the gate than the source and drain diffusion regions, wherein a portion of at least one of the extension regions is exposed at a surface of the body region by removing at least a part of one of the first and second sidewall spacers; and

a conductor formed at least in the exposed portion of the extension region, the conductor being in contact with the exposed portion of the extension region and at least a portion of the source diffusion region to form a Schottky diode.

35. The device according to claim 34 wherein the conductor contacts the body region.

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**APPENDIX B – EVIDENCE**

**NONE**

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## APPENDIX C - RELATED PROCEEDINGS

**NONE**